REMARKS

Claims 1-16 are pending in the present application. Claims 1-3, 6, 10 and 13-16 are amended above. New claims 17-24 are added above. No new matter is added by the claim amendments or new claims. Entry is respectfully requested.

The Applicant notes that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The specification is objected to at page 10, line 16 for informalities stated in the Office Action. The specification is amended above as suggested by the Examiner. Removal of the objection is respectfully requested.

Claims 1-15 stand rejected under 35 U.S.C. 112, second paragraph for reasons stated in the Office Action. The claims are amended above in a manner that is believed to overcome the rejections. Entry of the amendments and removal of the rejections are respectfully requested.

The Applicant notes, with appreciation, that the Office Action indicates at page 3 that claims 7-14 would be allowable if rewritten in independent form. Applicant wishes to defer submission of these claims pending consideration of the present amendment.

Claims 1-6 and 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Goto (U.S. Patent No. 6,535,902) in view of Miyamoto (U.S. Patent No. 6,043,675) and Bui (U.S. Patent No. 4,831,578). Reconsideration and removal of these rejections, and allowance of the claims, are respectfully requested.

Independent claim 1 as amended is directed to a 4-2 compressor for generating a sum bit and a carry bit as a result of four input data. A first logic circuit performs a NAND operation and a NOR operation of a first and a second input data, generates a first XOR/XNOR operation result

of the first and the second input data using the NAND operation result and NOR operation result, and generates a carry-out bit for a following stage by selecting either the NAND operation result or the NOR operation result in response to a third input data. A second logic circuit generates a second XOR/XNOR operation result of the third input data and a fourth input data, and generates a selection signal by selecting one of an XOR operation result and an XNOR operation result of the first XOR/XNOR operation result from the first logic circuit, in response to the second XOR/XNOR operation result. A third logic circuit generates the sum bit by selecting one of a carry-input bit and an inverted carry-input bit in response to the selection signal from the second logic circuit. A fourth logic circuit generates the carry bit by selecting one of the inverted carry-input bit and an inverted fourth input data in response to the selection signal from the second logic circuit.

Independent claim 16 as amended is directed to a 4-2 compressor for generating a sum bit and a carry bit as a result of four input data. A first XOR/XNOR logic circuit performs a NAND operation and a NOR operation of a first input data and a second input data, and generates a first XOR/XNOR operation result of the first input data and second input data by using the NAND operation result and the NOR operation result. A first multiplexer generates the carry-out bit for a following stage by selecting either the NAND operation result or the NOR operation result in response to an inverted third input data, wherein the first multiplexer is a single railed multiplexer. A second XOR/XNOR logic circuit performs a NAND operation and a NOR operation of a third input data and fourth input data, and generates a second XOR/XNOR operation result of the third input data and fourth input data by using the NAND and NOR operation results. A second multiplexer generates a selection signal by selecting either the XOR operation result or the XNOR operation result from the first XOR/XNOR logic circuit, in response to the second XOR/XNOR operation result from the second XOR/XNOR logic circuit, wherein the second multiplexer is a dual railed multiplexer. A third multiplexer generates the sum bit, by selecting one of a carry-input bit and inverted carry-input bit, in response to the selection signal from the second multiplexer, wherein the third multiplexer is a single railed multiplexer. A fourth multiplexer generates the carry bit, by selecting one of an inverted fourth

input data and the inverted carry-input bit, in response to the selection signal from the second multiplexer, wherein the fourth multiplexer is a single railed multiplexer.

In the present invention as claimed in amended independent claim 1, a "first logic circuit" generates a "carry-out bit" for a following stage "by selecting either the NAND operation result or the NOR operation result in response to a third input data." This feature of the present invention is described at least in connection with Fig. 6 of the present specification, which shows a first logic circuit 110 generating a carry-out bit C_{out} by selecting either the NAND operation result or the NOR operation result of the first input data I_1, and the second input data I_2 generated by the first XOR/XNOR logic circuit (see, for example, element 52 of Fig. 6 of the specification). The selection is made in response to a third input data I_3 (see specification, page 12, lines 2-5). In addition, a second logic circuit (see, for example, element 120 of Fig. 6 of the specification) generates a selection signal by selecting "one of an XOR operation result and an XNOR operation result of the first XOR/XNOR operation result" (see, for example, element 64 of Fig. 6 of the specification) from the first logic circuit in response to the second XOR/XNOR operation result generated at the output of logic gate 54 (see, for example, specification, page 7, lines 4-11).

Similarly, in the present invention as claimed in amended claim 16, "a first multiplexer" generates a "carry out bit" for a following stage "by selecting either the NAND operation result or the NOR operation result in response to an inverted third input data, wherein the first multiplexer is a single railed multiplexer." In addition, "a second multiplexer" generates a selection signal "by selecting either the XOR operation result or the XNOR operation result from the first XOR/XNOR logic circuit, in response to the second XOR/XNOR operation result from the second XOR/XNOR logic circuit, wherein the second multiplexer is a dual railed multiplexer."

Goto is cited in the Office Action at paragraph 3 as disclosing the invention "substantially as claimed." However, close inspection of Goto reveals that Goto fails to teach or suggest "a first logic circuit...for generating a carry-out bit for a following stage by selecting either the

NAND operation result or the NOR operation result in response to a third input data", as claimed in independent claim 1. Instead, Goto's 4-2 compression circuit (see Goto, Fig. 16) provides a transfer gate 402 to output a third data signal x3 as the carry-out signal Cout when the EOR circuit 430(133) output is true, and provides a transfer gate 401 to output the output of the NAND circuit 422 as the carry-out signal Cout when the EOR circuit 430(133) output is false (see Goto, Fig. 16, page 10, lines 1-10, and page 10, lines 40-44). Since Goto's 4-2 compression circuit outputs either a third input signal x3 or the output of the NAND circuit 422, it follows that Goto does not output "the NAND operation result or the NOR operation result" of inputs X1 and X2 as the "carry-out bit", as claimed in amended independent claim 1. Moreover, the Goto circuit selects either a third data signal x3 or the output of the NAND circuit 422 as the carry-out signal Cout in response to the output of the EOR circuit 430(133), and not in response to the Goto third data signal x3. Therefore, the Goto circuit does not make the selection in response to "a third input data", as claimed in independent claim 1.

In addition, it is submitted that Goto fails to teach or suggest "a second logic circuit...for generating a selection signal by selecting one of an XOR operation result and an XNOR operation result of the first XOR/XNOR operation result from the first logic circuit in response to the second XOR/XNOR operation result", as claimed in amended independent claim 1. With reference to Fig. 16 of Goto, transfer gates 405, 406 generate a selection signal (output from transfer gates 405, 406) by selecting either the result (x3 $\oplus$ x4) (input to transfer gate 405 and output of EOR circuit 440 at inverter 415) or the result (/ (x3 $\oplus$ x4)) (input to transfer gate 406 and output of EOR circuit 440 at transfer gate 404) in response to the output of EOR/ENOR circuit 430(133) (constructed from elements 421, 422, 423, and 412). Goto therefore does not generate "a selection signal by selecting one of an XOR operation result and an XNOR operation result of the first XOR/XNOR operation result from the first logic circuit", and further does not generate the selection signal "in response to the second XOR/XNOR operation result", as claimed in amended independent claim 1.

Miyamoto is cited in the Office Action at page 2 as disclosing "logic circuits using NAND & NAND/AND or NOR & NOR/OR for generating XOR/XNOR." Bui is cited in the Office Action at page 3 as disclosing "a logic circuit having a 'third data' Carry-in for selecting either NAND operation result or NOR operation result." However, like Goto, neither reference teaches or suggests "a first logic circuit...for generating a carry-out bit for a following stage by selecting either the NAND operation result or the NOR operation result in response to a third input data", as claimed in amended independent claim 1. In addition, like Goto, neither reference teaches or suggests "a second logic circuit...for generating a selection signal by selecting one of an XOR operation result and an XNOR operation result of the first XOR/XNOR operation result from the first logic circuit in response to the second XOR/XNOR operation result", as claimed in amended independent claim 1. Therefore, there is no combination of Goto, Miyamoto, and Bui that would provide such a teaching or suggestion. Accordingly, it is respectfully submitted that claim 1 is allowable over the combined teachings of the cited references. Reconsideration and removal of the rejection of claim 1 are respectfully requested.

With regard to amended independent claim 16, it is submitted that the cited Goto, Miyamoto, and Bui references, taken alone or in combination, fail to teach or suggest "a first multiplexer" generating "the carry-out bit for a following stage by selecting either the NAND operation result or the NOR operation result in response to an inverted third input data, wherein the first multiplexer is a single railed multiplexer", as claimed in amended independent claim 16. Nor does the combination teach or suggest "a second multiplexer for generating a selection signal by selecting either the XOR operation result or the XNOR operation result from the first XOR/XNOR logic circuit, in response to the second XOR/XNOR operation result from the second XOR/XNOR logic circuit, wherein the second multiplexer is a dual railed multiplexer", as claimed in amended independent claim 16.

It is therefore submitted that independent claims 1 and 16 are in condition for allowance, and such allowance is respectfully submitted. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which

they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: July 28, 2004

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
J:\SAM\0231\072804 amend\amendmenta.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant